AV9110

Integrated Circuit Systems, Inc.

Serially Programmable Frequency Generator

General Description

The **AV9110** generates user specified clock frequencies using an externally generated input reference, such as 14.318 MHz or 10.00 MHz crystal connected between pins 1 and 14. Alternately, a TTL input reference clock signal can be used. The output frequency is determined by a 24-bit digital word entered through the serial port. The serial port enables the user to change the output frequency on-the-fly.

The clock outputs utilize CMOS level output buffers that operate up to 130 MHz.

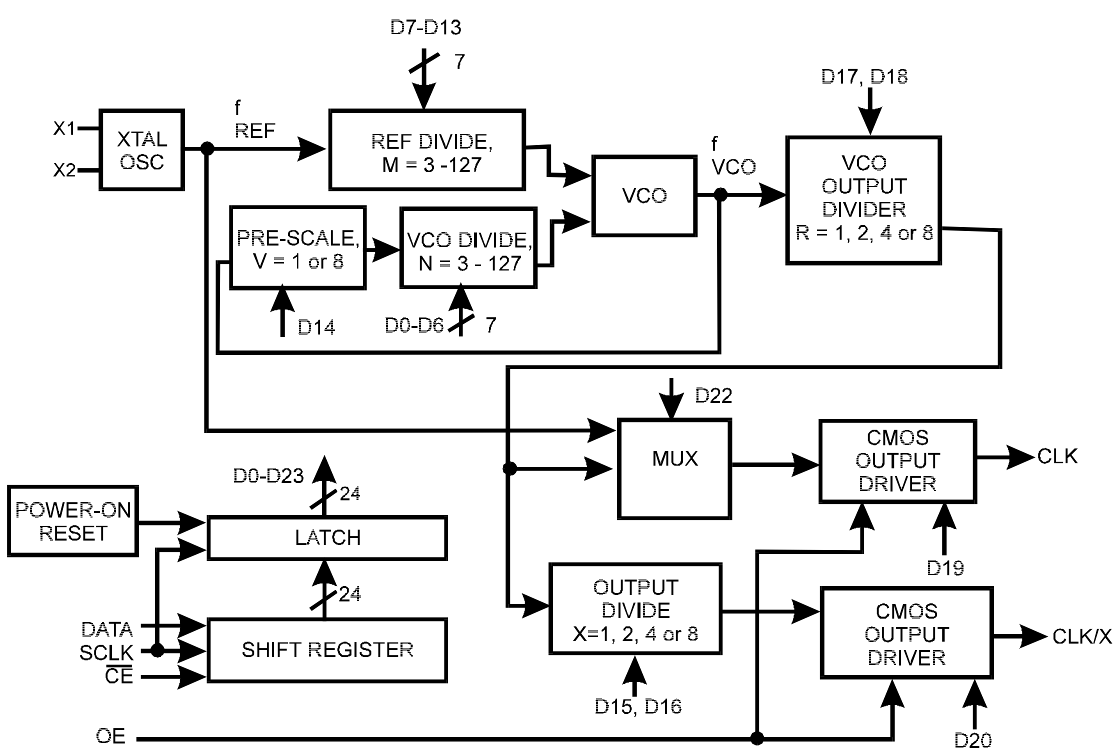
Features

- Complete user programmability of output frequency through serial input data port
- On-chip Phase-Locked Loop for clock generation
- Generates accurate frequencies up to 130 MHz
- Tristate CMOS outputs
- 5 volt power supply
- Low power CMOS technology
- 14-pin DIP or 150-mil SOIC
- Very low jitter
- Wide operating range VCO

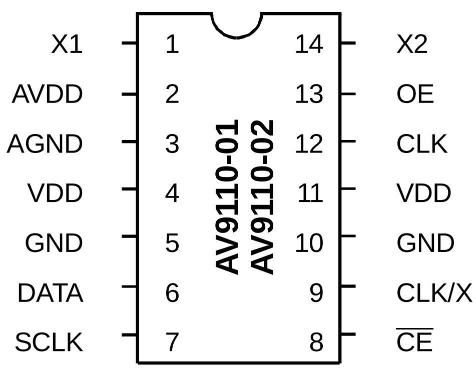
Applications

Graphics: The **AV9110** generates low jitter, high speed pixel (or dot) clocks. It can be used to replace multiple expensive high speed crystal oscillators. The flexibility of this device allows it to generate non-standard graphics clocks, allowing the user to program frequencies on-the-fly.

Block Diagram



Pin Configuration



14-Pin DIP, SOIC

Clock Reference Implementations:

AV9110-01 vs. AV9110-02

The **AV9110** requires a stable reference clock (5 to 32 MHz) to generate a stable, low-jitter output clock. The **AV9110-**01 is optimized to use an external quartz crystal as a frequency reference, without the need of additional external components. The **AV9110-**02 is optimized to accept an TTL clock reference. Either device can be used with an external crystal or accept a TTL clock reference, although extra components may be required. The various combinations implied are summarized in Figure 2 (see page 7).

Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	DESCRIPTION
1	X1	Input	Crystal input or TTL reference clock.
2	AVDD	Power	ANALOG power supply. Connect to +5V.
3	AGND	Power	ANALOG GROUND.
4	VDD	Power	Digital power supply. Connect to +5V.
5	GND	Power	Digital GROUND.
6	DATA	Input	Serial DATA pin.
7	SCLK	Input	SERIAL CLOCK. Clocks shift register.
8	$\overline{CE}$	Input	CHIP ENABLE. Active low, controls data transfer.
9	CLK/X	Input	CMOS CLOCK divided by X output.
10	GND	Power	Digital GROUND.
11	VDD	Power	Digital power supply. Connect to +5V.
12	CLK	Output	CMOS CLOCK output.
13	OE	Input	OUTPUT ENABLE. Tristates both outputs when low.
14	X2	Input	Crystal input or TTL reference clock.

Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias. . . . . 0°C to +70°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to V_{DD} + 0.5V
Power dissipation . . . . 0.8 Watts
Storage temperature . . . . -65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = +5V±10%, T_A = 0°C to 70°C unless otherwise stated

DC/STATIC						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD} = 5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD} = 5V	2.0	-	-	V
Input Low Current	I_{IL}	V_{IN} = OV	-	-	-5	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}	-	-	5	µA
Output Low Voltage[1]	V_{OL}	I_{OL} = 8mA	-	-	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH} = 8mA	2.4	-	-	V
Input Clock Rise Time[1]	$ICLK_r$		-	-	20	ns
Input Clock Fall Time[1]	$ICLK_f$		-	-	20	ns
Supply Current	I_{DD}	No load	-	25	-	mA
AC/DYNAMIC						
Output frequency range	f_o		0.78	-	130	MHz
Rise time, 20-80%[1]	t_r	25pF load	-	-	3	ns
Fall time, 80-20%[1]	t_f	25pF load	-	-	3	ns
Duty cycle[1]	d_t	25pF load	40	-	60	%
Jitter, 1 sigma[1]			-	±40	-	ps
Jitter, absolute[1]			-	±125	-	ps
Input reference freq.; AV9110-01[1]	f_{REF}	Crystal input	5	14.318	32	MHz
Input reference freq.; AV9110-02[1]	f_{REF}	TTL input	0.6	14.318	32	MHz
Input DATA or SCLK frequency[1]	f_{DATA}		-	-	32	MHz
Skew, Output to Output/X[1]	t_{skew}		-	400	-	ps

Note:
1. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Serial Programming

The **AV9110** is programmed to generate clock frequencies by entering data through the shift register. Figure 1 displays the proper timing sequence. On the negative going edge of $\overline{CE}$, the shift register is enabled and the data at the DATA pin is loaded into the shift register on the rising edge of the SCLK. Bit D0 is loaded first, followed by D1, D2, etc. This data consists of the 24 bits shown in the Shift Register Bit Assignment in Table 1, and therefore takes 24 clock cycles to load.

An internal counter then disables the input and transfers the data to internal latches on the rising edge of the 24th cycle of the SCLK. Any data entered after the 24th cycle is ignored until $\overline{CE}$ must remain low for a minimum of 24 SLCK clock cycles. If $\overline{CE}$ is taken high before 24 clock cycles have elapsed, the data is ignored (no frequency change occurs) and the counter is reset. Tables 1 and 2 display the bit location for generating the output clock frequency and the output divider circuitry, respectively.

Table 1: Shift Register Bit Assignment

BIT	ASSIGNMENT	EQUATION VARIABLE	DEFAULT -01	DEFAULT -02	BIT
0	VCO frequency divider (LSB)	N Integer	1	1	0
1	"		1	1	1
2	"		1	1	2
3	"		1	1	3
4	"		1	1	4
5	"		1	1	5
6	VCO frequency divider MSB)		1	1	6
7	Reference frequency divider	M Integer	0	0	7
8	"		1	1	8
9	"		0	0	9
10	"		0	0	10
11	"		1	1	11
12	"		0	0	12
13	Reference frequency divider		0	0	13
14	VCO pre-scale divide (0=divide by 1, 1= divide by 8		0	0	14
15	CLK/X output divide COD0 (see Table 2)	V	0	1	15
16	CLK/X output divide COD1 (see Table 2)	X	1	0	16
17	VCO output divide VOD0 (see Table 2)		0	0	17
18	VCO output divide VOD1 (see Table 2)		1	1	18
19	Output enable CLK (0=tristate)	R	1	1	19
20	Output enable CLK/X (0=tristate)		1	1	20
21	Reserved. Should be programmed high (1)		1	1	21
22	Reference clock select on CLK (1 = reference frequency)		0	0	22
23	Reserved. Should be programmed high (1)		1	1	23

Output Divider Truth Tables

Table 2

COD1	COD0	CLK/X Output Divide (X)
0	0	1
0	1	2
1	0	4
1	1	8

Table 3

VOD1	VOD0	VCO Output Divide (R)
0	0	1
0	1	2
1	0	4
1	1	8

Programming the PLL

The AV9110 has a wide operating range but it is recommended that it is operated within the following limits:

2 MHz < f_{REF} < 32 MHz	f_{REF} = Input reference frequency
200 kHz < $\frac{f_{REF}}{M}$ < 5 MHz	M = Reference divide, 3 to 127
50 MHz < f_{VCO} < 250 MHz	f_{VCO} = VCO output frequency
f_{VCO} < 250 MHz	f_{CLK} = CLK or CLK/X output frequency

The AV9110 is a classical PLL circuit and the VCO output frequency is given by:

$$f_{VCO} = \frac{N \bullet V \bullet f_{REF}}{M}$$

where N = VCO divided, 3 to 127
M = Reference divide, 3 to 127
V = Prescale, 1 or 8

The 2 output drivers then give the following frequencies:

$$f_{CLK} = \frac{f_{VCO}}{R} = \frac{N \bullet V \bullet f_{REF}}{M \bullet R}$$ or f_{REF} (output muxable by bit 17)

$$f_{CLK/X} = \frac{f_{VCO}}{R \bullet X} = \frac{f_{VCLK}}{X}$$ Where R, X = output dividers 1, 2, 4 or 8

Notes:
1. Output frequency accuracy will depend solely on input reference frequency accuracy.
2. For output frequencies below 125 MHz, it is recommended that the VCO output divide, R, should be 2 or greater. This will give improved duty cycle.
3. The minimum output frequency step size is approximately 0.2% due to the divider range provided.

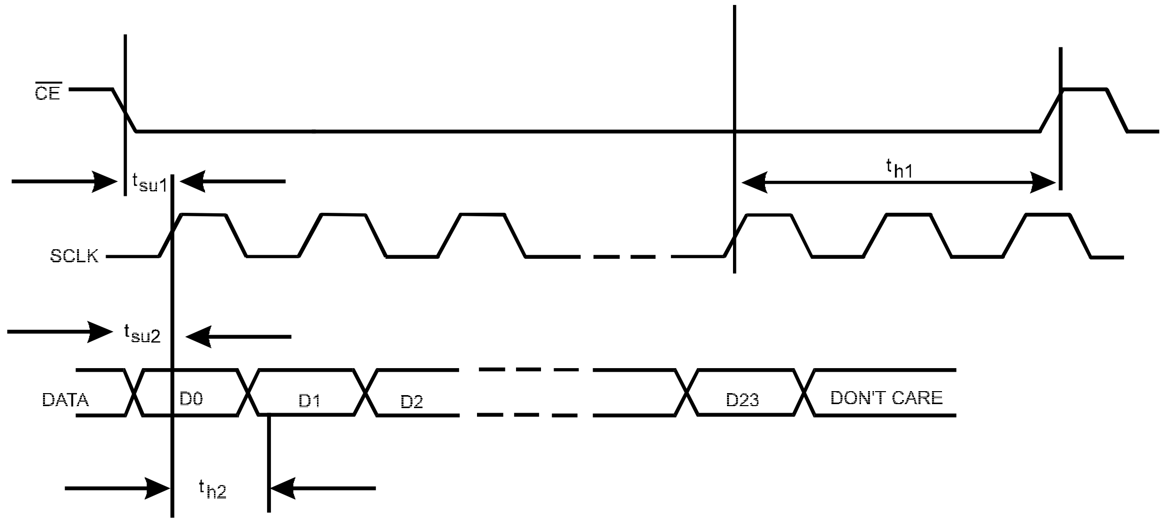


Figure 1 - Serial Programming

AC Timing

Parameter	Minimum time (ns)
t_{su1}	10
t_{su2}	10
t_{h1}	10
t_{h2}	10

Frequency Acquisition Time

Frequency acquisition (or "lock") time is the time that it takes to change from one frequency to another, and is a function of the difference between the old and new frequencies. The **AV9110** can typically lock to within 1% of a new frequency in less than 200µs. This is also true with power-on.

Power-On Reset

Upon power-up the internal latches are preset to provide the following output clock frequencies (14.318 MHz reference assumed):

Device	CLK output	CLK/X output
AV9110-01	25.175 MHz	6.29 MHz
AV9110-02	25.175 MHz	12.59 MHz

These preset default frequencies can be changed with a custom metal mask, as can other attributes.

Jitter

For high performance applications, the **AV9110** offers extremely low jitter and excellent power supply rejection. The one sigma jitter distribution is typically less than ±125ps. For optimum performance, the device should be decoupled with both a 2.2µF and a 0.1µF capacitor. Refer to Recommended Board Layout diagram on page 8.

Output Enable

The **AV9110** outputs can be disabled with either the OE pin or through serial programming. Setting the OE pin low tristates CLK and CLK/X. Alternatively, setting bits D19 and D20 low in the serial word will tristate the two outputs. Both the OE pin and D19 or D20 must be high to enable an output.

Frequency Transition Glitches

The **AV9110** starts changing frequency on the rising edge of the 24th serial clock. If the programming of any output divider is changed, the output clock may glitch before locking to the new frequency in less than 200µs with no output glitches (no partial clock cycles).

AV9110 Quartz Crystal Selection

When an external quartz crystal will be used as a frequency reference for the AV9110, attention needs to be given to crystal selection if accurate reference frequency and output frequency is desired. The AV9110 uses a Pierce oscillator design which operates the quartz crystal in parallel-resonant mode. It requires a quartz crystal cut for parallel-resonant operation to ensure an accurate frequency of oscillation (a less expensive series-resonant crystal can be used with the device but it will oscillate approximately 0.1% too fast). The AV9110-01 has internal crystal load capacitors which result in a total crystal load capacitance of approximately 12pF±10%. The AV9110-02 does not have internal load capacitors, but contributes about 3pF load capacitance to the crystal.

Following is a list of recommended crystal devices for the AV9110. They have been tested by the crystal manufacturer to operate suitably with the AV91xx-series crystal oscillator design, having load capacitance characteristics that are compatible with the AV9110-01.

Toyocom

Part Number
TN4-30374. . . . . . . 14.318 MHz surface mount crystal
TN4-30375. . . . . . . 20 MHz surface mount crystal
TN4-30376. . . . . . . 14.318 MHz through-hole crystal
TN4-30377. . . . . . . 20 MHz through-hole crystal

Epson

Part Number
MA-505 or . . . . . . Surface mount crystal
MA-506
CA-301. . . . . Through-hole crystal

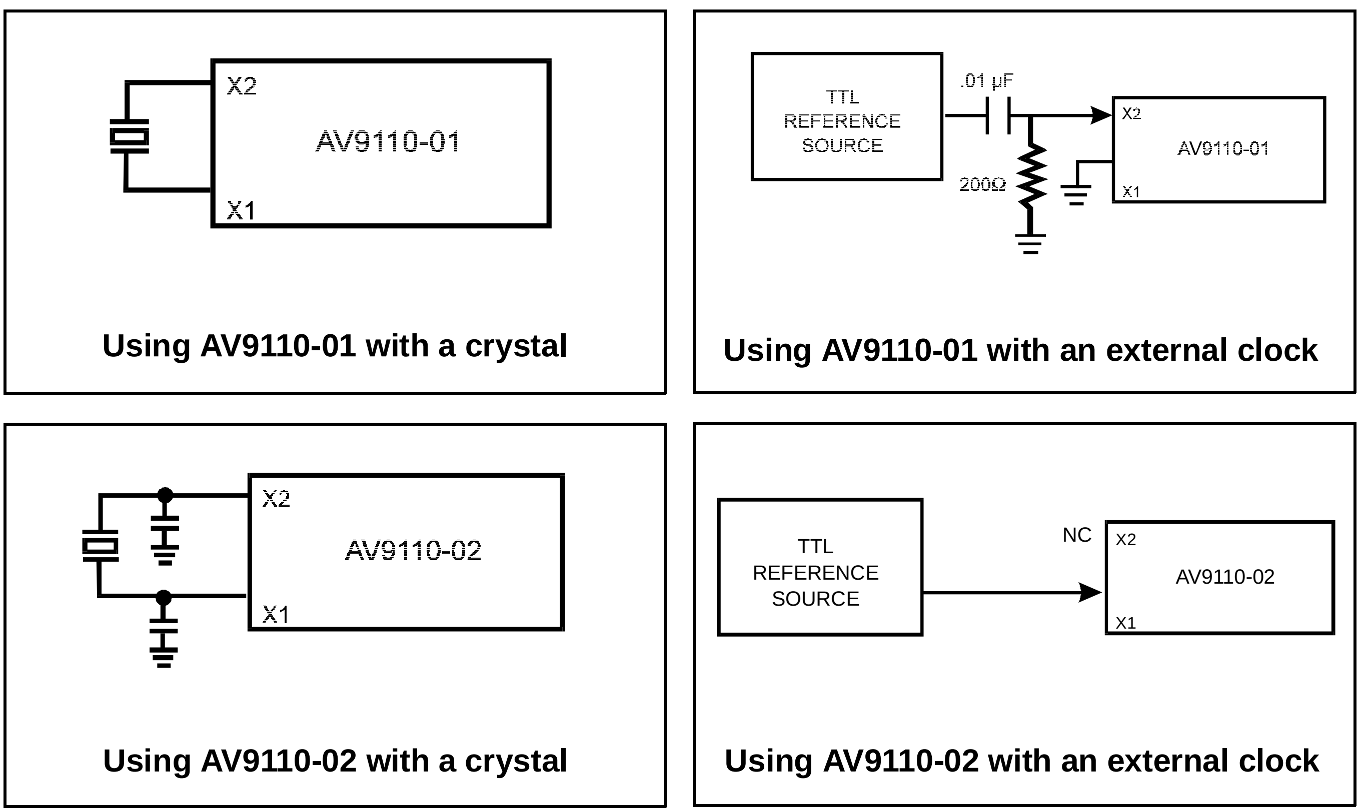
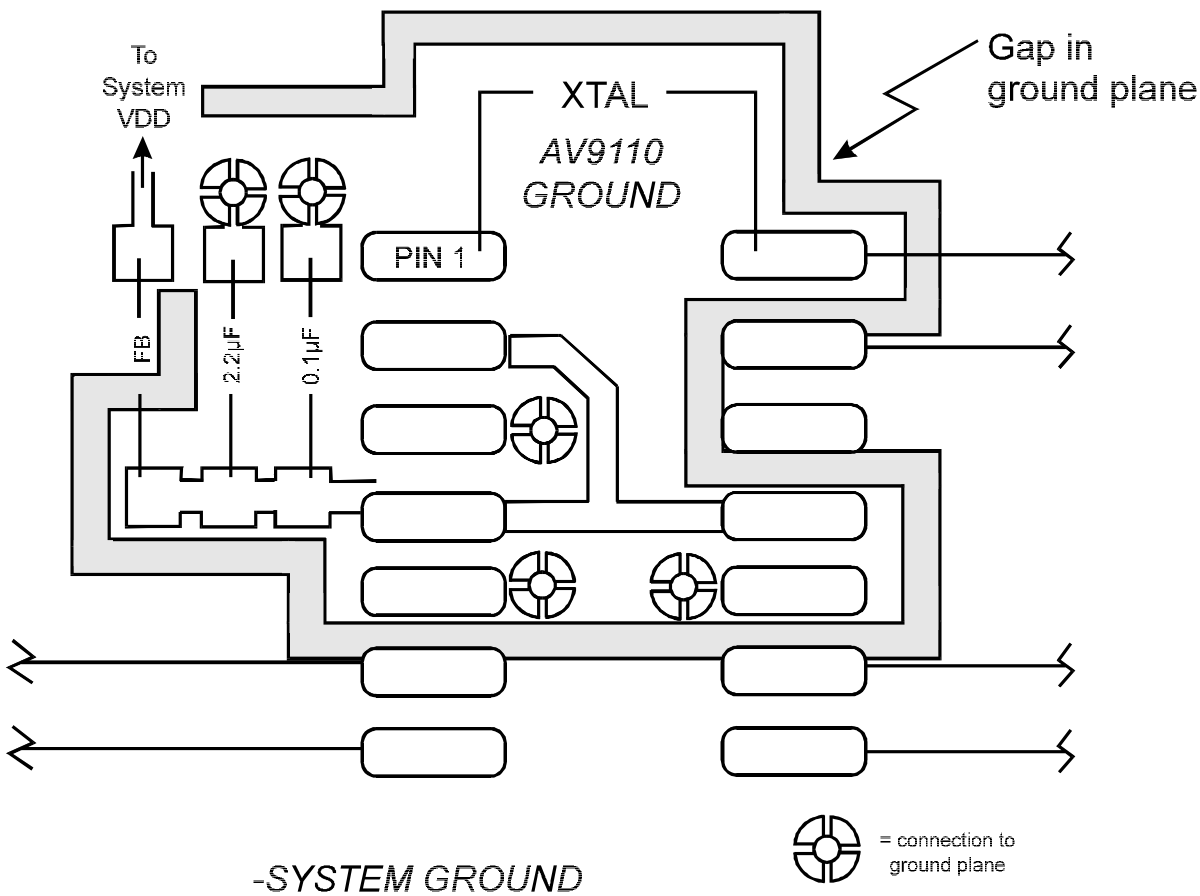


Figure 2 - Clock Reference Combinations

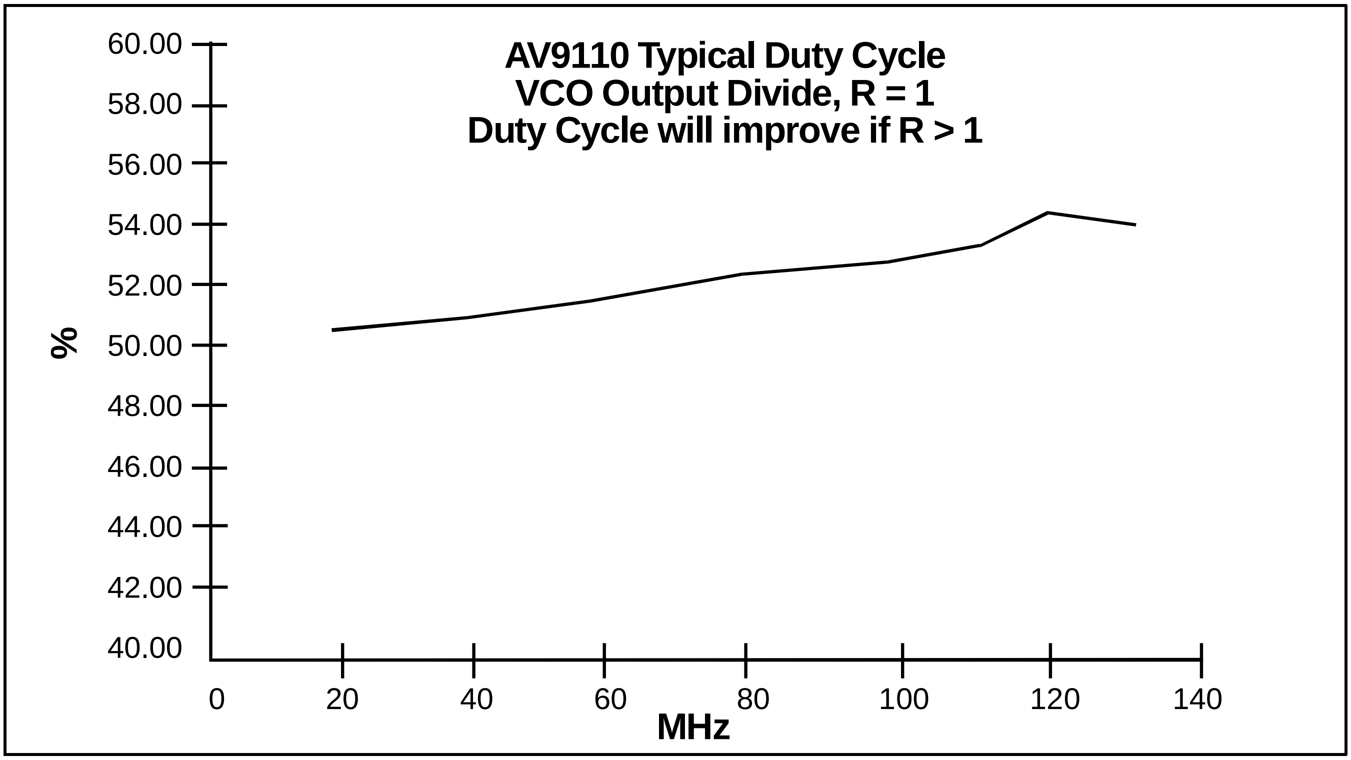
AV9110 Recommended Board Layout

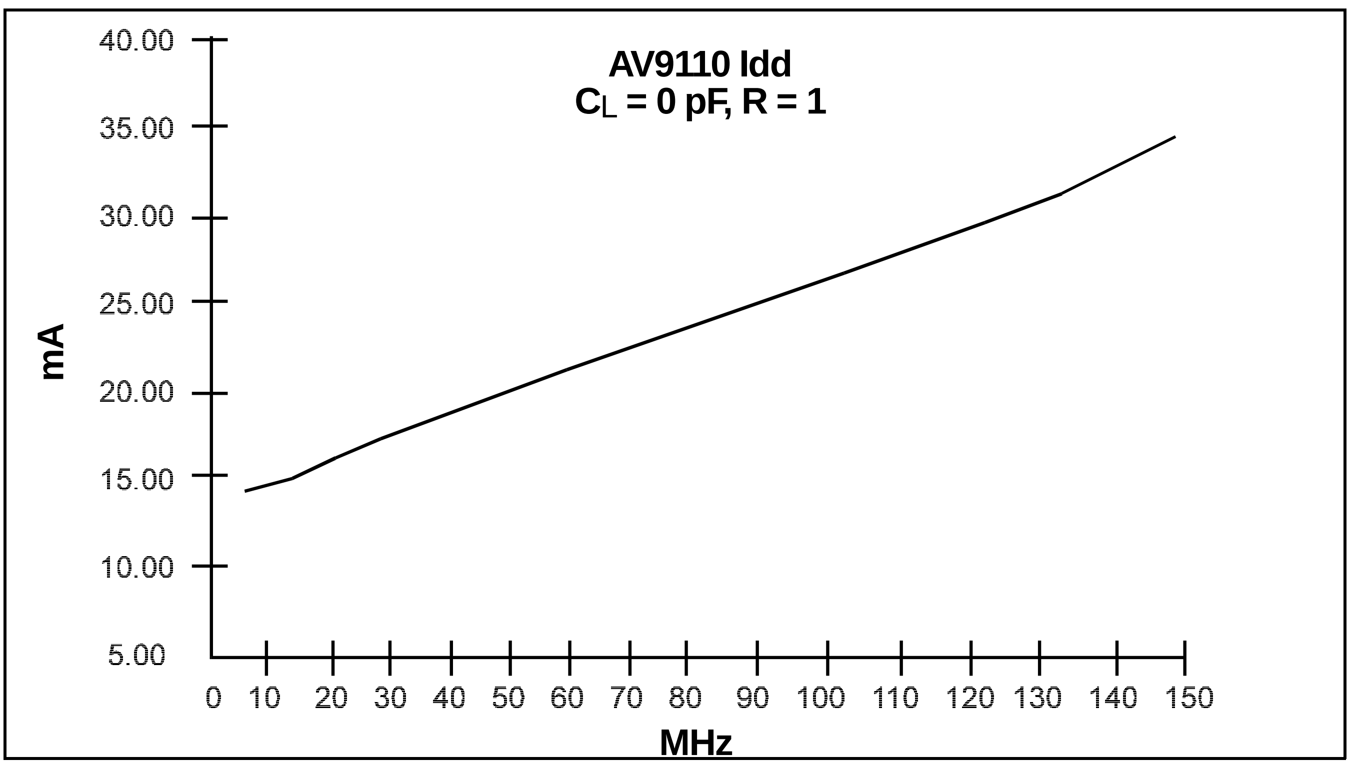


This is the recommended layout for the **AV9110** to maximize clock performance. Shown are the power and ground connections, the ground plane, and the input/output traces.

Use of the isolated ground plane and power connection, as shown, will prevent stray high frequency ground and system noise from coupling to the **AV9110**. As when compared to using the system ground and power planes, this technique will lessen output clock jitter. The isolated ground plane should be connected to the system ground plane at one point near the 2.2mF decoupling cap. For lowest jitter performance, the isolated ground plane should be kept away from clock output pins and traces. Keeping the isolated ground plane area as small as possible will minimize EMI radiation. Use a sufficient gap between the isolated ground plane and system ground plane to prevent AC coupling. The ferrite bead in the VDD line is optional, but will help reduce EMI.

The traces to distribute the output clocks should be over an unbroken system ground or power supply plane. The trace width should be about two times the thickness of the PC board between the trace and the underlying plane. These guidelines help minimize clock jitter and EMI radiation. The traces to distribute power should be as wide as possible.


AV9110 Typical Duty Cycle
VCO Output Divide, R = 1
Duty Cycle will improve if R > 1
%
60.00
58.00
56.00
54.00
52.00
50.00
48.00
46.00
44.00
42.00
40.00
0
20
40
60
80
100
120
140
MHz


AV9110 Idd
CL = 0 pF, R = 1
mA
40.00
35.00
30.00
25.00
20.00
15.00
10.00
5.00
0
10
20
30
40
50
60
70
80
90
100
110
120
130
140
150
MHz

Ordering Information

AV9110-01CN14, AV9110-02CN14

Example:

ICS XXXX-PPP M X#W

Lead Count
Lead Count=1, 2 or 3 digits

Package Type
N=DIP

Pattern Number (2 or 3 digit number for parts with ROM code patterns, if applicable)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

AV9110-01CS14, AV9110-02CS14

Example:

ICS XXXX-PPP M X#W

Lead Count
Lead Count=1, 2 or 3 digits

Package Type
S=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns, if applicable)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device